Update on big.LITTLE on TC2

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Agenda

- big.LITTLE Software solutions overview
- ARM's Test Chip 2 overview
- Benchmarking Methodology and Use Cases
- IKS status update
- big.LITTLE MP status update

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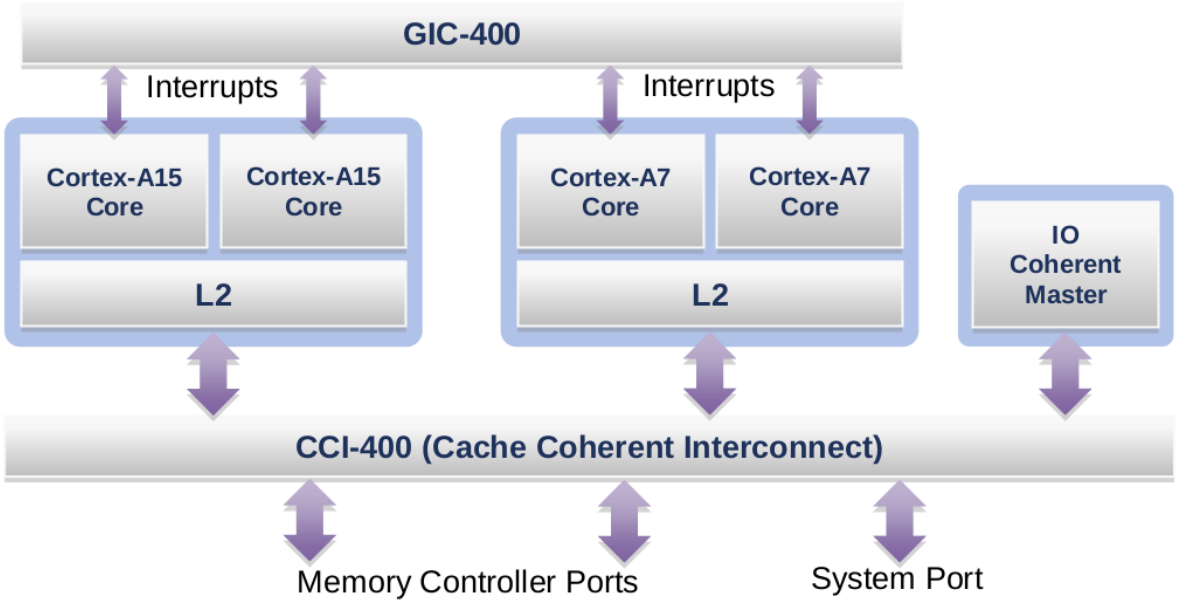
big.LITTLE overview

- Performance and power efficiency in one system:



	Cortex-A15 vs Cortex-A7 Performance	Cortex-A7 vs Cortex-A15 Energy Efficiency
Dhrystone	1.9x	3.5x
FDCT	2.3x	3.8x
IMDCT	3.0x	3.0x
MemCopy L1	1.9x	2.3x
MemCopy L2	1.9x	3.4x

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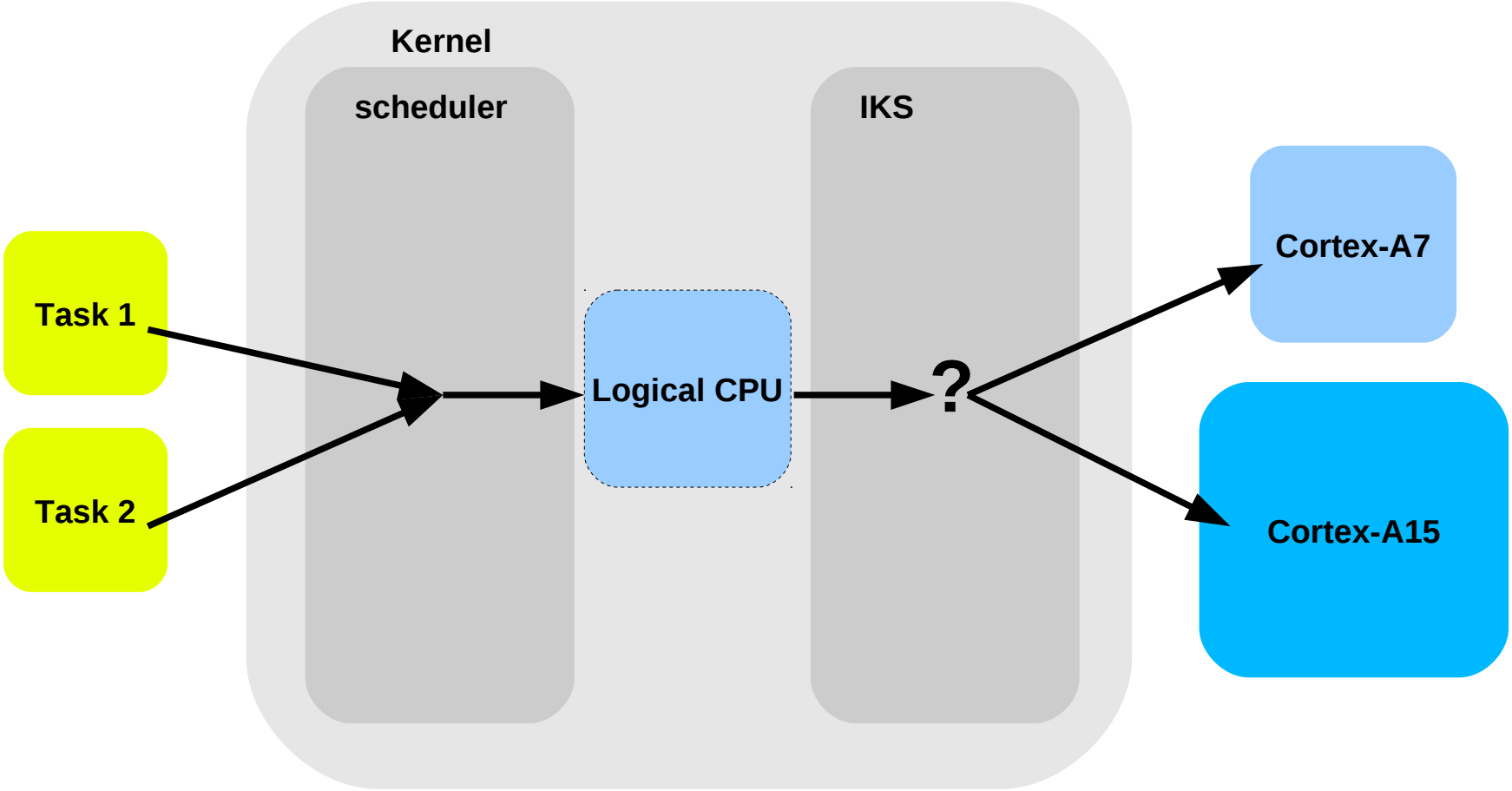
IKS solution – Basics

- In-Kernel Switcher (IKS):
  - Targeted first generation big.LITTLE products.



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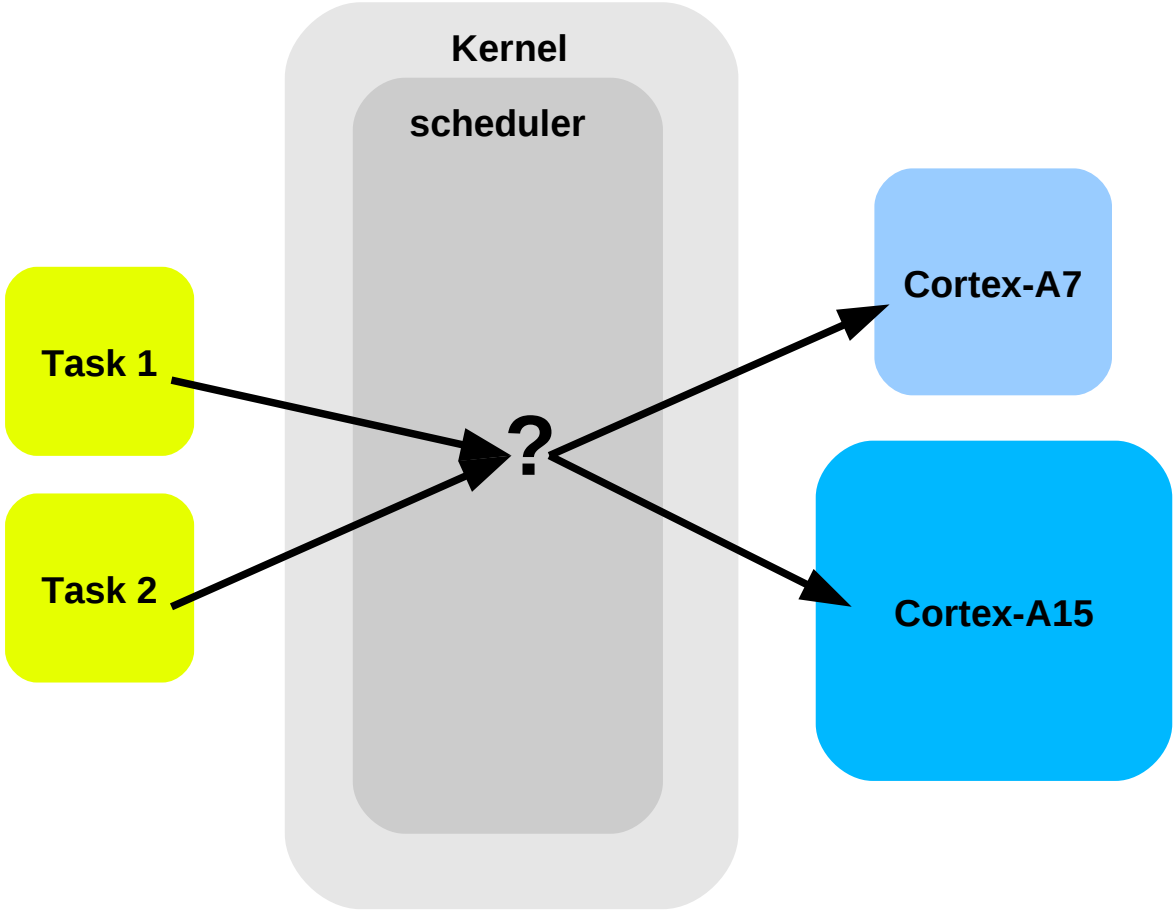
MP solution



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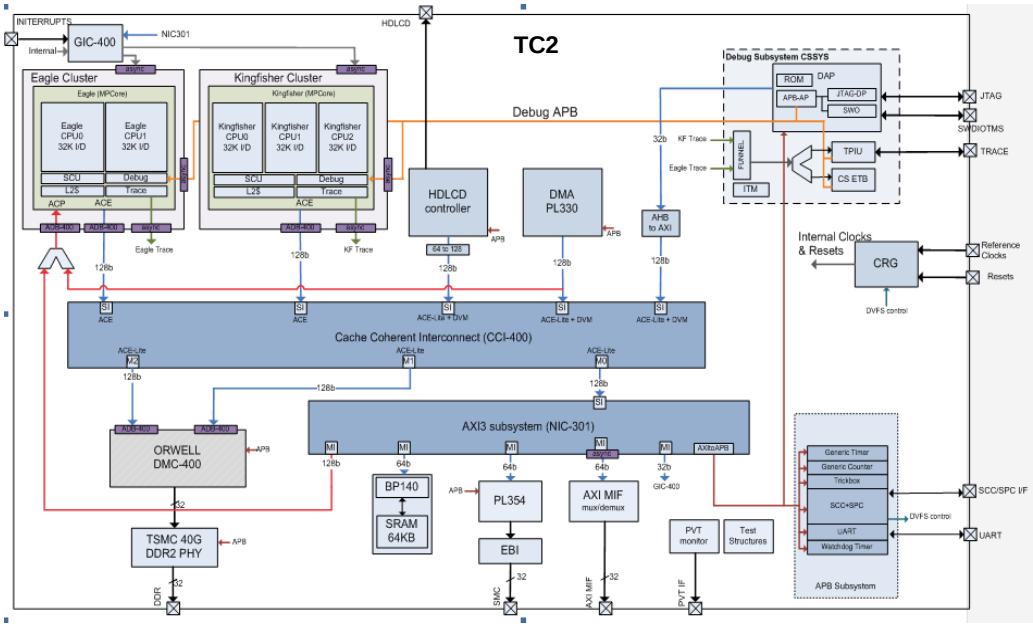
ARM's Test Chip 2 (TC#2): An Overview



- A Versatile Express core tile publically available:
  - Capabilities
    - 2 x A15 (r2p1) @ up to 1.2 Ghz
    - 3 x A7 (r0p1) @ up to 1Ghz
    - CCI/DMC/GIC/ADB (r0p0)
    - DMA (PL330)
      - 2GB external DDR2 memory @ 400Mhz
    - 64k internal SRAM
  - Coresight debug (including JTAG and ITM trace but no STM)
  - No GPU
  - cpufreq support: Independent for each cluster with limited voltage scaling
  - cpuidle support: Cluster power gating

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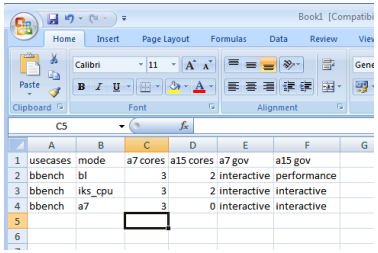
Benchmarking Methodology



usecases	mode	a7 cores	a15 cores	a7 gov	a15 gov
bbench	bl	3	2	interactive	performance
bbench	iks_cpu	3	2	interactive	interactive
bbench	a7	3	0	interactive	interactive

CSV config:
- Use case
- Scheduling model
- Numbers of cores to use
- Scaling governors

Results

Performance
Power
Configurable:
- CCI
- ftrace
- streamline

- Automated system for running user workloads on target device

Choose workload

Choose CPU mode:
Cortex-A7, Cortex-A15, Migration (cluster or CPU), or MP

Choose active cores in each cluster
TC2: 1-2 big, 1-3 LITTLE

Choose DVFS governor:
Interactive, performance, powersave, ondemand

Extensible – parameterisation

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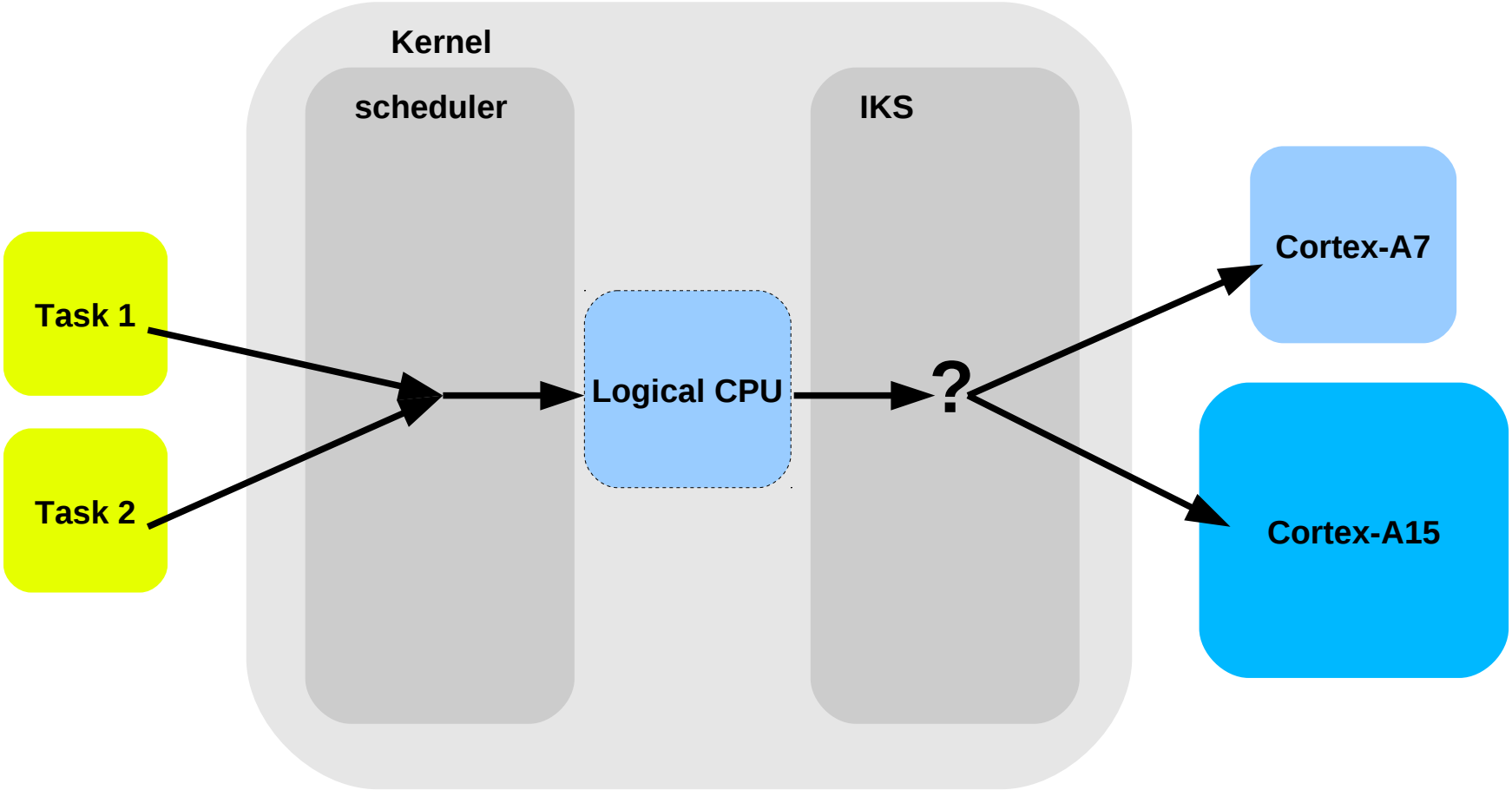
IKS solution

- Targeted first generation big.LITTLE products.



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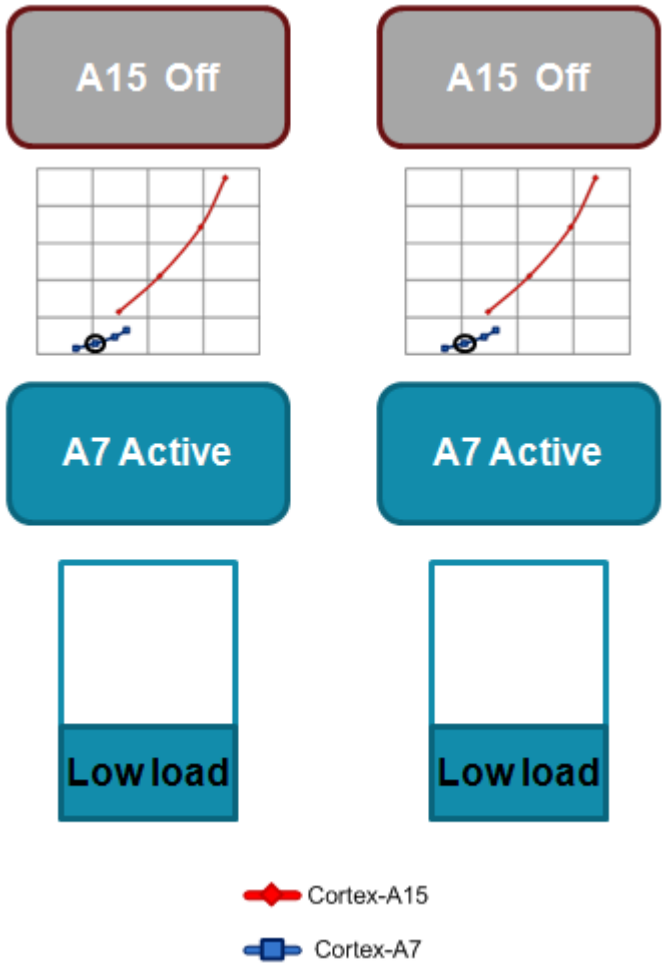
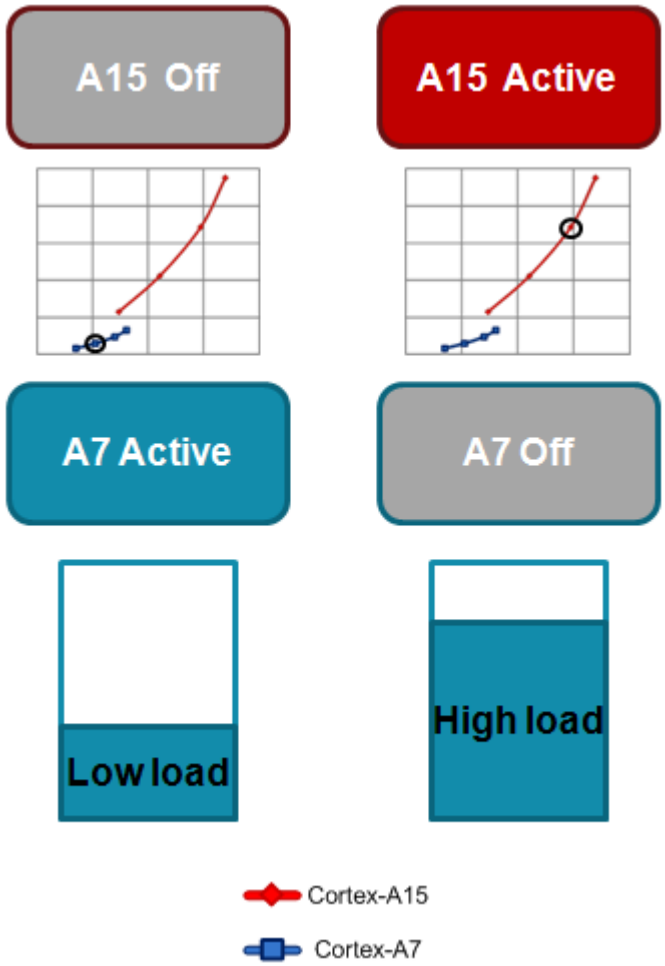
IKS: CPU Migration



- big.LITTLE extends DVFS
- DVFS algorithm monitors load on each CPU
- When load is low it can be handled on a LITTLE processor
- When load is high the context is transferred to a big processor
- The unused processor can be powered down
- When all processors in a cluster are inactive the cluster and its L2 cache can be powered down

IKS: CPU Migration



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IKS: OPP mapping to A7 / A15 on TC2

- Virtual Frequency maps OPPs to big or LITTLE cores

	Virtual OPP	Physical OPP A7	Physical OPP A15	Voltage
A7	350000	350000		V1
	400000	400000		V1
	... X	X		V1
	800000	800000		V1
	900000	900000		V2
	1000000	1000000		V3
A15	1200000		600000	V1
	1400000		700000	V1
	... X		2X	V1
	2000000		1000000	V1
	2200000		1100000	V2
	2400000		1200000	V3

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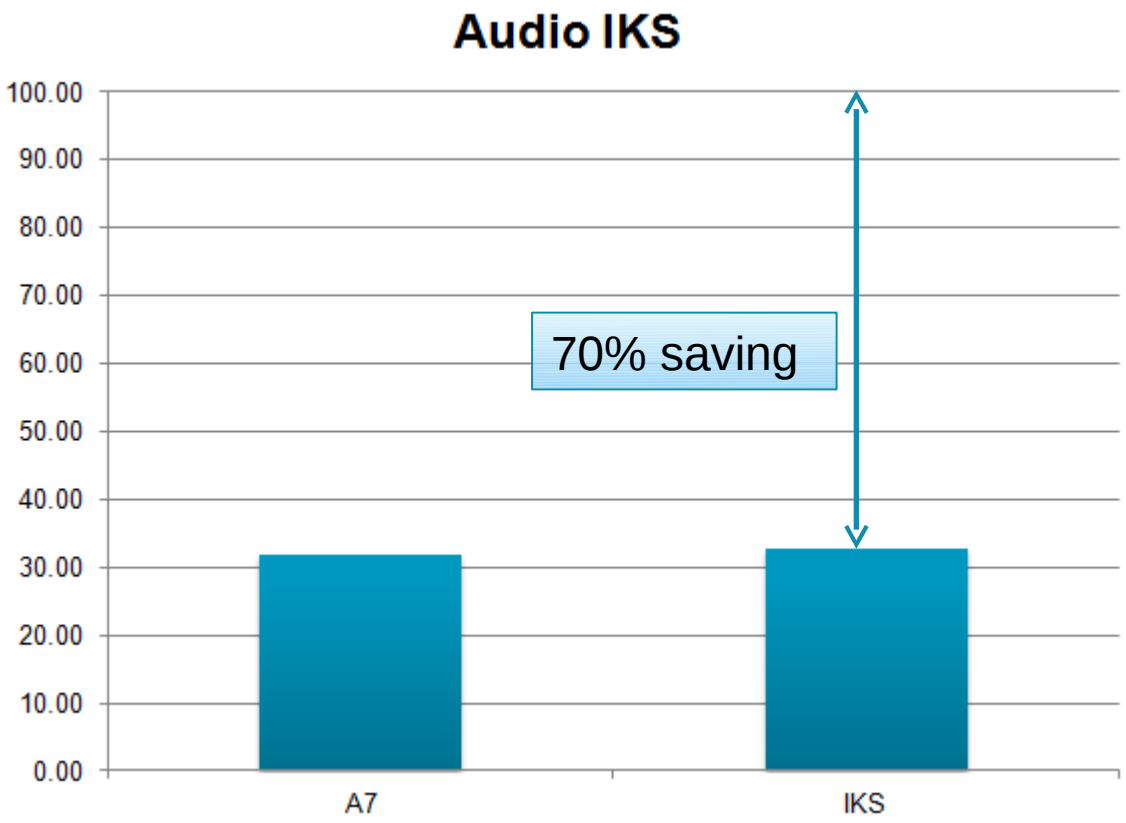
IKS: Results for Audio on TC2



TC2:
A15 up to 1.2 GHz
A7 up to 1 GHz
Better results expected on representative silicon.

- Power compared to executing the use case on A15
- IKS does not use A15s during Audio run

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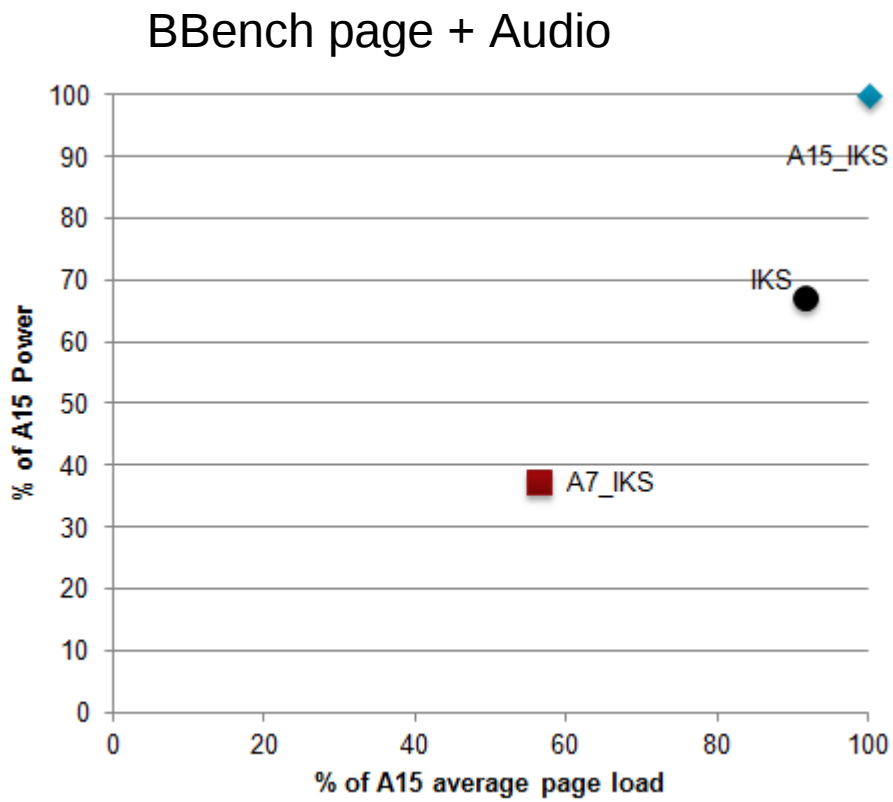
IKS: Results for BBench + Audio on TC2



TC2:
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A7 up to 1 GHz
Better results expected on representative silicon.

- Performance is measured as from page loading times of BBench
- Results normalised to power and performance consumed on same use case run on A15 only

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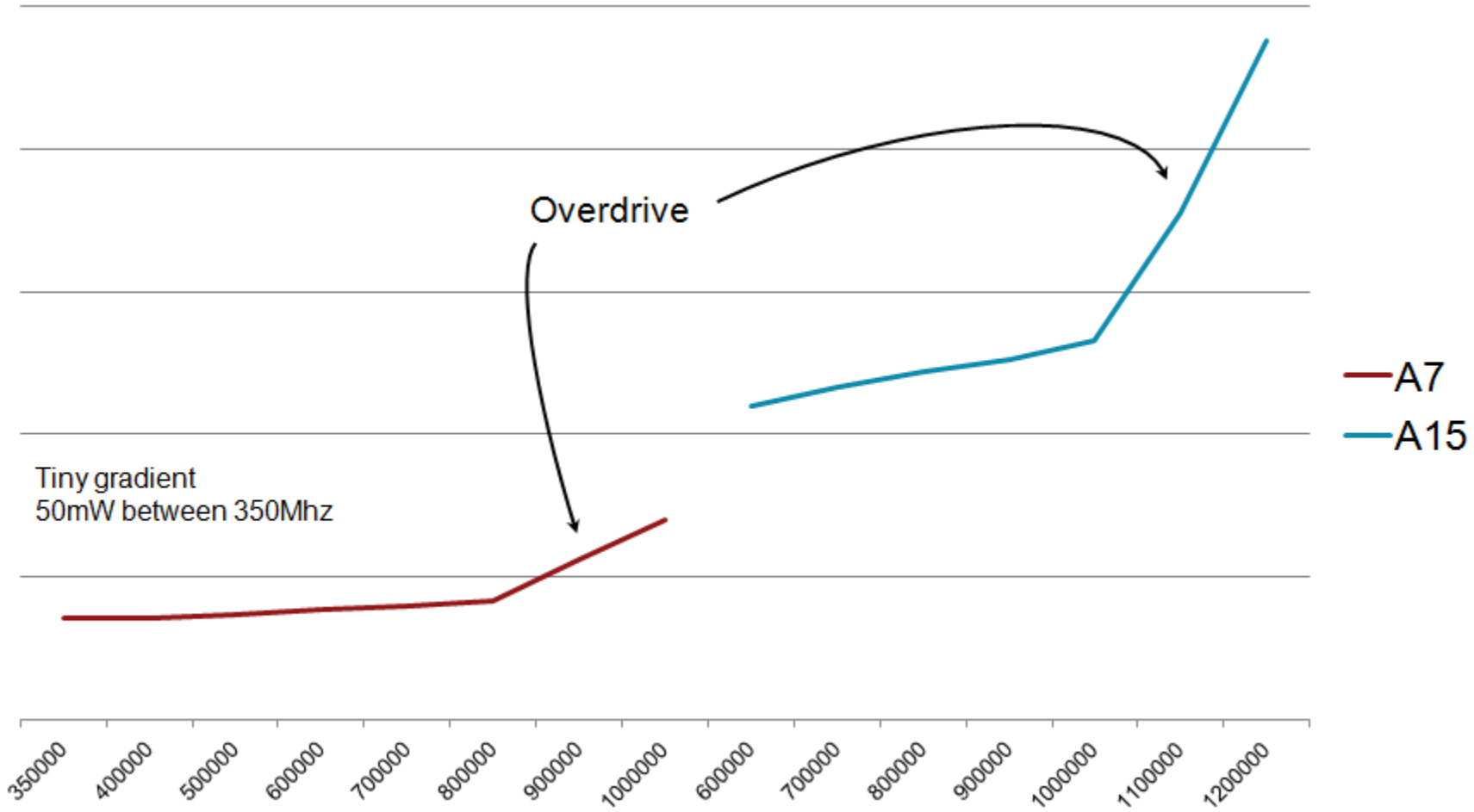
IKS: OPPs on TC2



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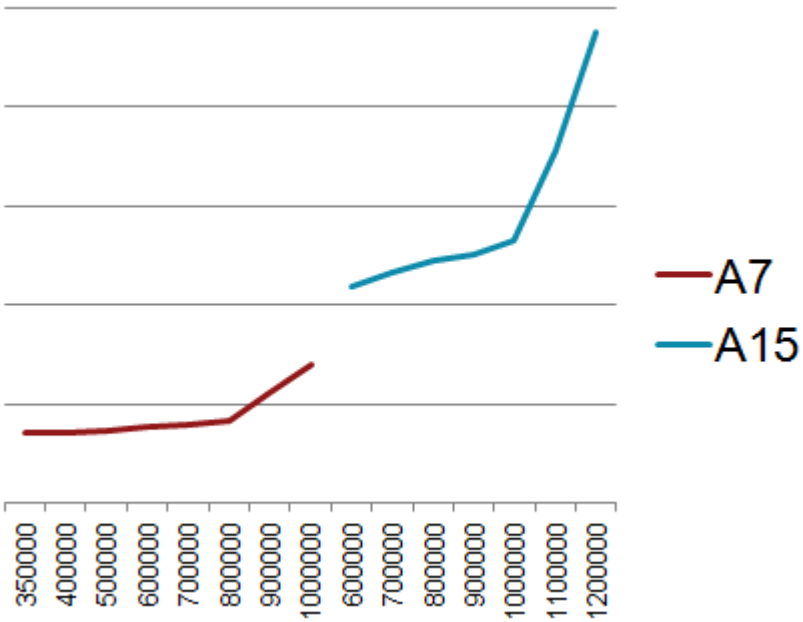
IKS: Interactive governor on TC2




```
if (cpu_load >= go_hispeed_load){
    ...
    new_freq = max_freq * cpu_load / 100;
    ...
    }
else {
    ...
    new_freq = hispeed_freq*cpu_load/100;
    ...
    }
```

- For A15 on TC2 with a go_highspeed at 85% (default) this algorithm only uses overdrive section of A15
- Approach is to introduce a second point of inflection:highspeed2

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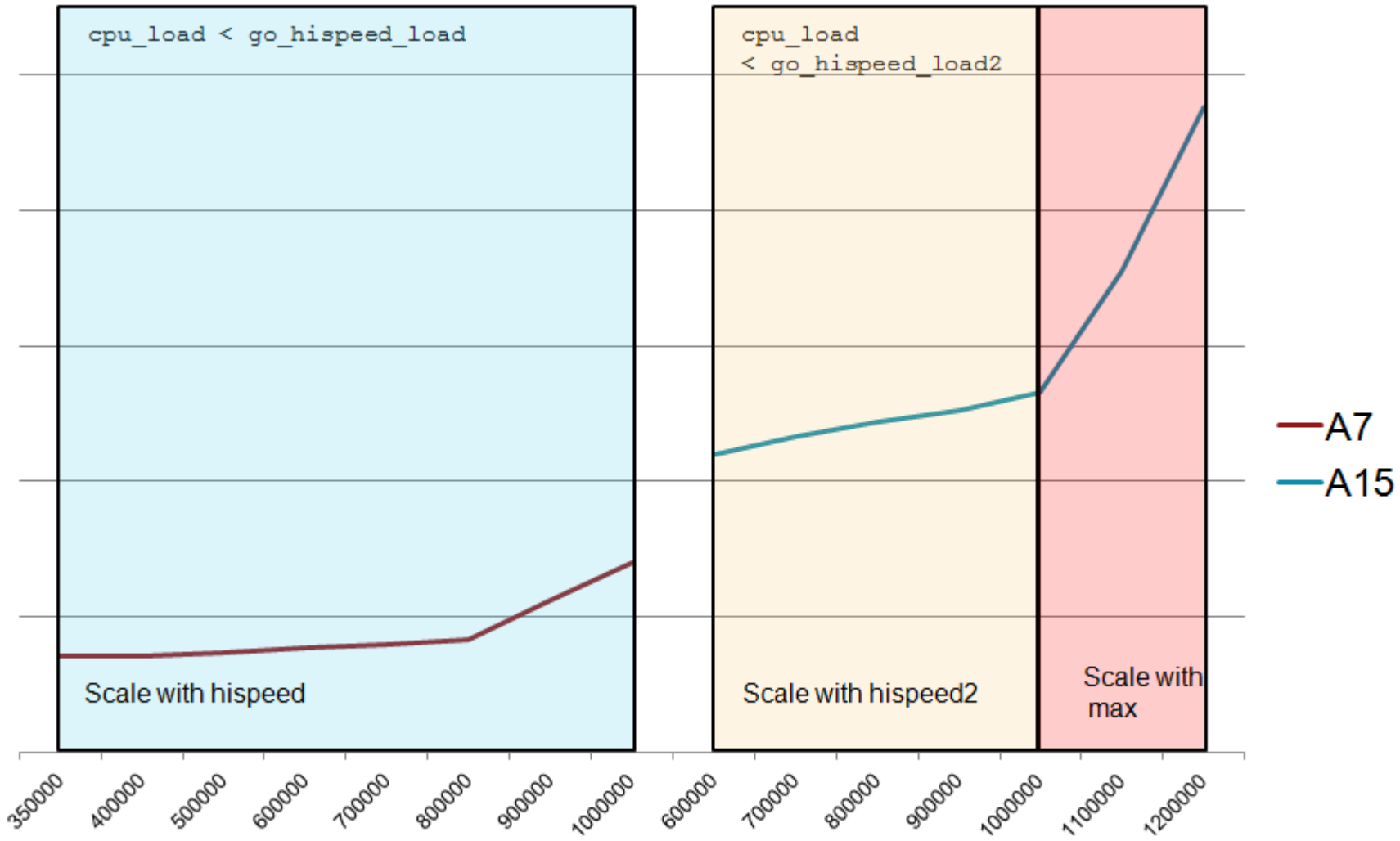
IKS: Hispeed2



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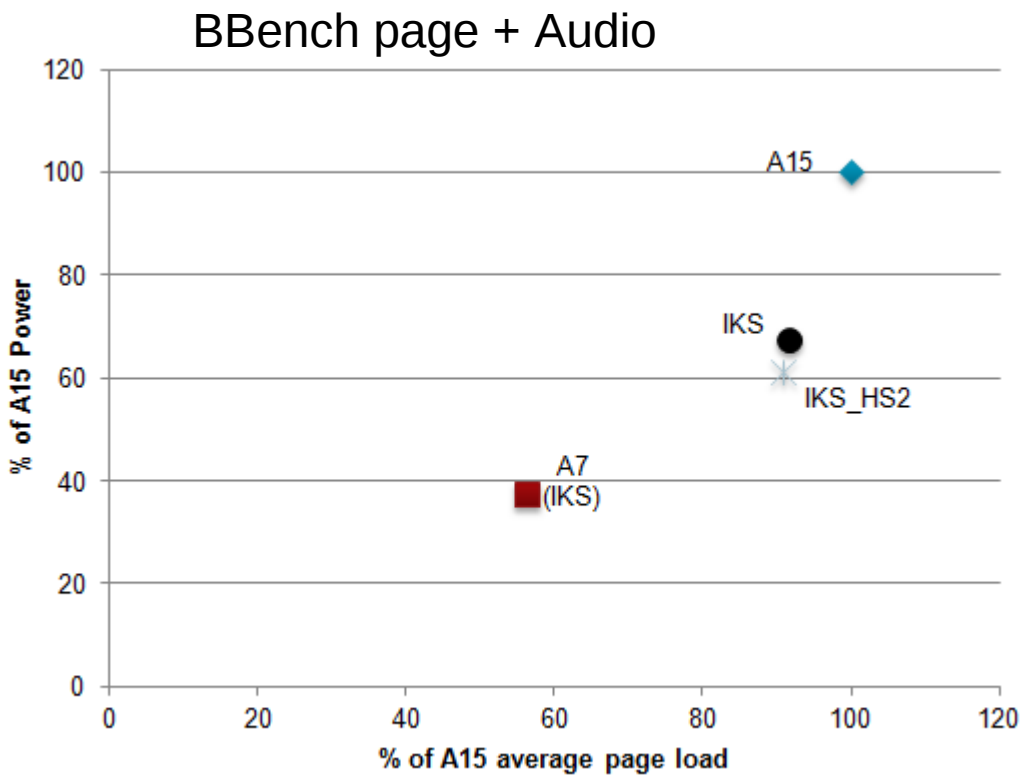
IKS: Results: Bbench + Audio



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A15 up to 1.2 GHz
A7 up to 1 GHz
Better results expected on representative silicon.

- Power improves with no performance cost

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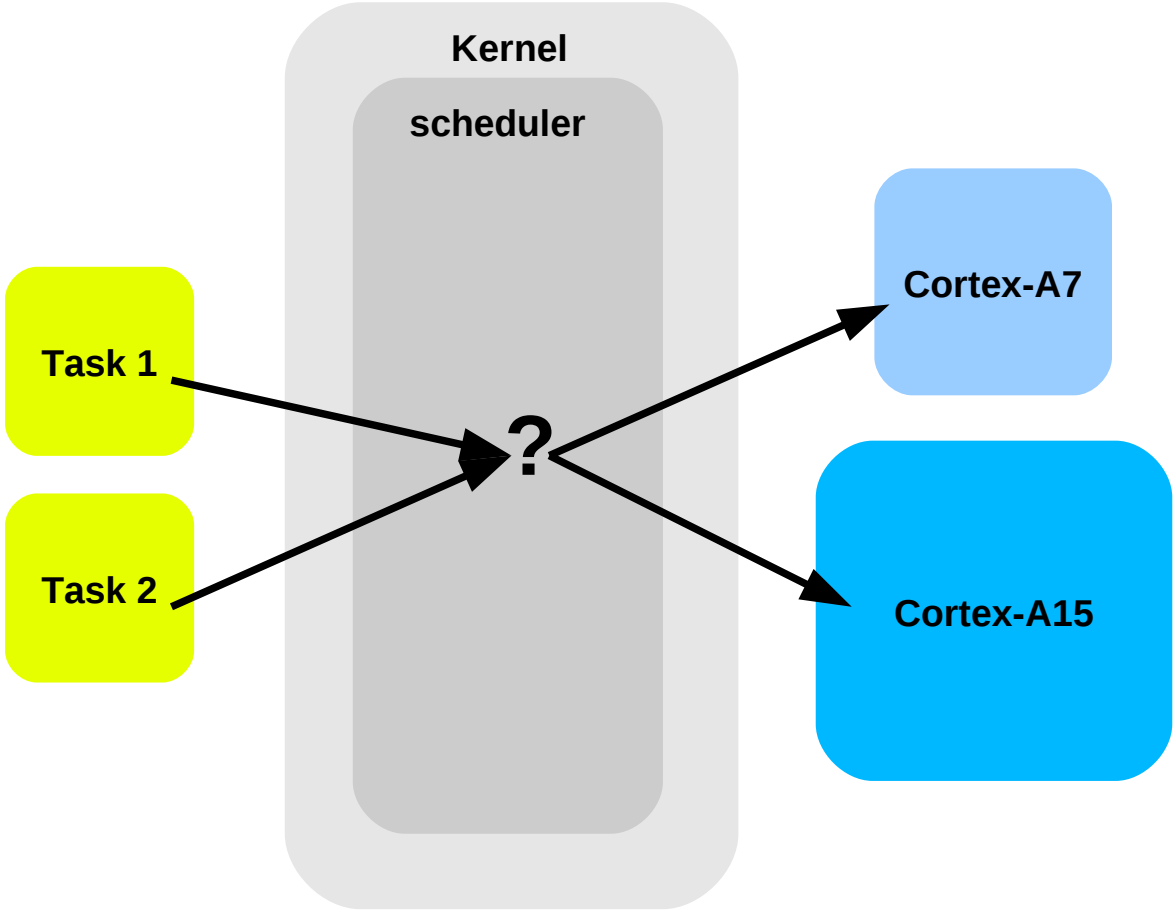
MP solution



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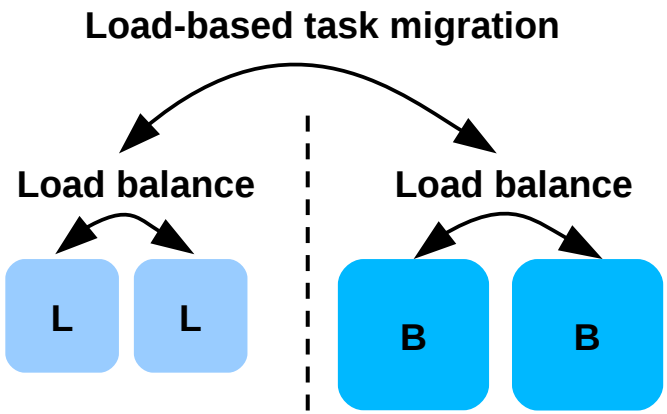
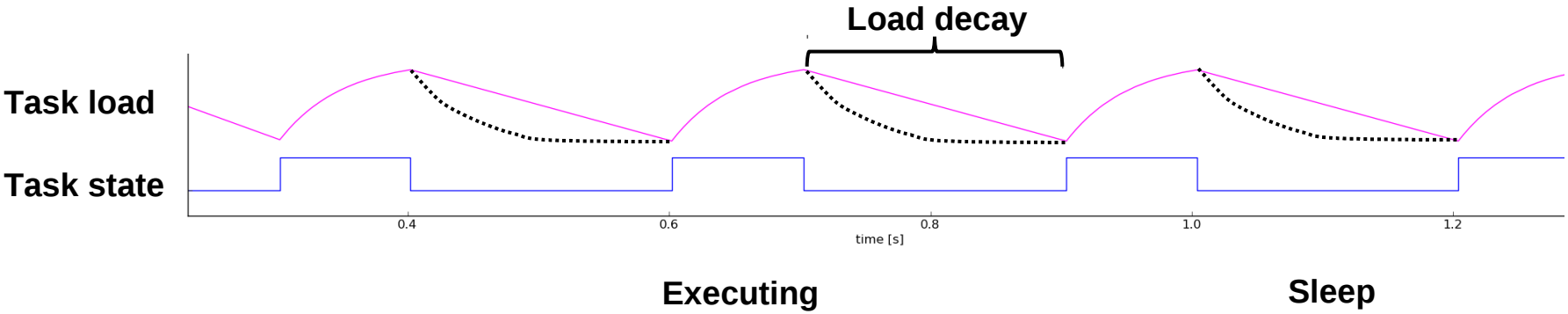
MP solution – more details

- Scheduler modifications:
  - Treat big and LITTLE cpus as separate scheduling domains.
  - Use PJT's load-tracking patches to track individual task load.
  - Migrate tasks between the big and the LITTLE domains based on task load.
  - Patch set available through Linaro.





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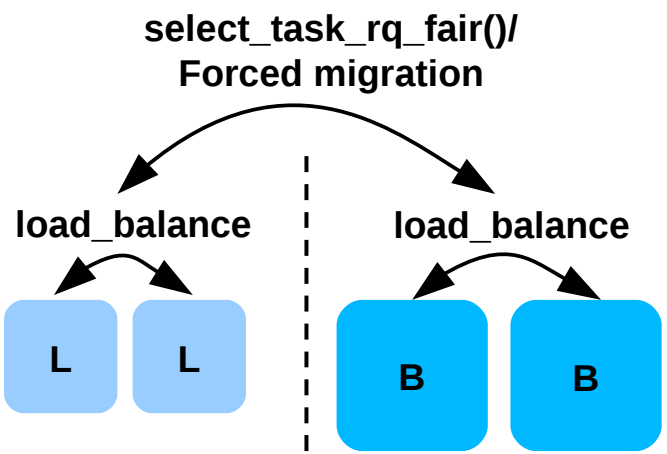
MP: Experimental Implementation

- Scheduler modifications:
  - Apply PJTs' load-tracking patch set.
  - Set up big and little sched_domains with no load-balancing between them.
  - select_task_rq_fair() checks task load history to select appropriate target CPU for tasks waking up.
  - Add forced migration mechanism to push of the currently running task to big core similar to the existing active load balancing mechanism.
  - Periodically check (run_rebalance_domains()) current task on little runqueues for tasks that need to be forced to migrate to a big core.



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MP: ARM TC2: Audio

- Workload: Audio (mp3 playback)
- Performance/Energy target:
  - A7 energy
- Status:
  - Audio related task do not use A15s, but the power consumption is still significantly more than A7 alone.
- MP not as power efficient as IKS yet
- Todo:
  - Target spurious wake-ups on A15. All the extra power comes from the A15's which shouldn't be used at all.

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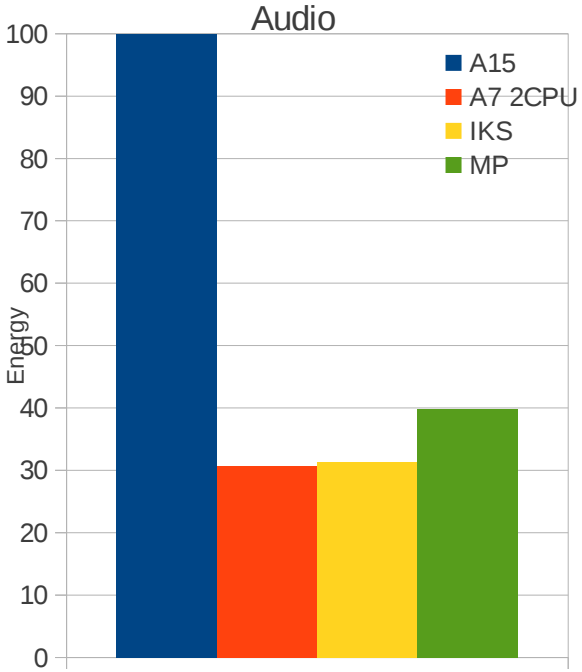
Better results expected on representative silicon.



	Energy
A7	30.79%
MP	39.86%

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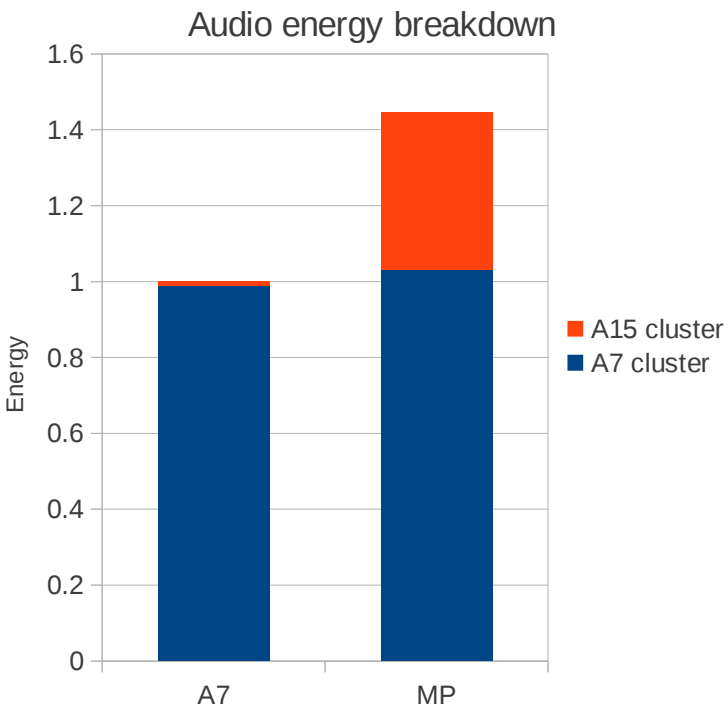
MP: Audio workload analysis

- Where is the extra energy spent with MP?
  - Need a look at why A15's consume power when they are not necessary.

Enter idle	cpu0	cpu1	cpu2	cpu3	cpu4
0	6	2	2379	260	423
1	801	807	8316	9373	9652

hrtimer functions	cpu0	cpu1	cpu2	cpu3	cpu4
hrtimer_wakeup	2	2	1212	417	190
tick_sched_timer	404	58	483	507	779

WQ functions	cpu0	cpu1	cpu2	cpu3	cpu4
vmstat_update	30	2	27	25	28
cache_reap	15	2	14	13	14
phy_state_machine	31	0	0	0	0



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Better results expected on representative silicon.

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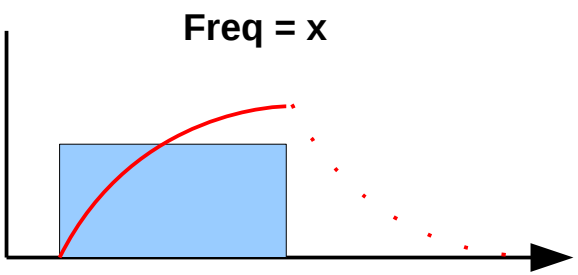
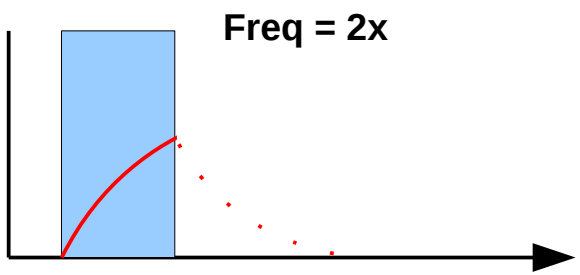
Scale invariant load

- Load accumulation rate does not scale with available compute capacity (frequency, big/LITTLE cpu)
- Currently, there is no link between cpufreq and the scheduler
  - Tasks may be migrated away from a cpu at low frequency by the scheduler before cpufreq has increased the frequency to match the cpu load.
- Scaling the tracked load accumulation to match the current frequency mitigates this issue.
  - Tasks cannot accumulate enough load at low frequency to trigger migration and must wait for cpufreq to react first.





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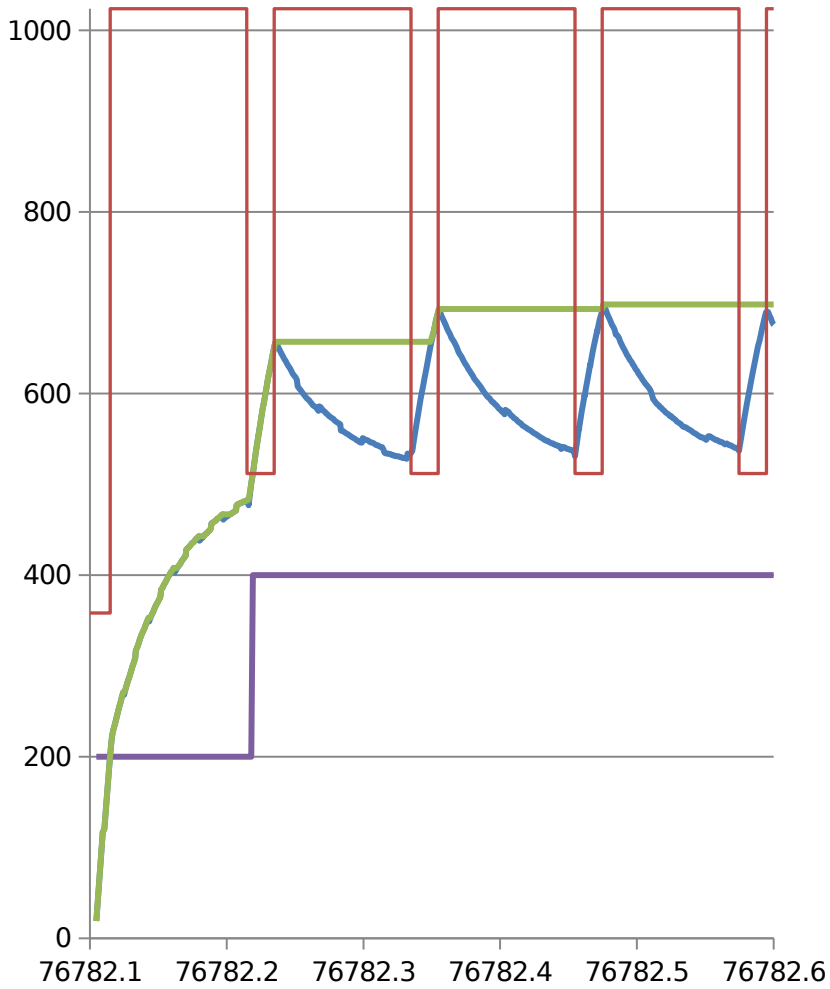
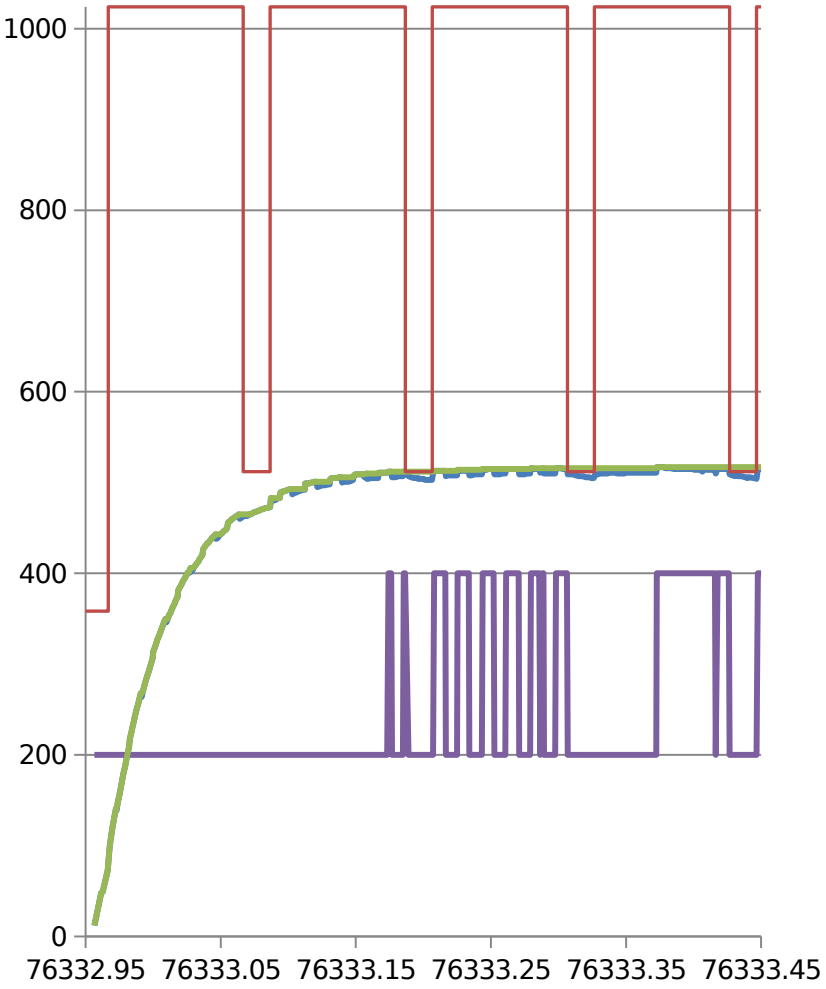
Scale invariant load

Original



Frequency invariant



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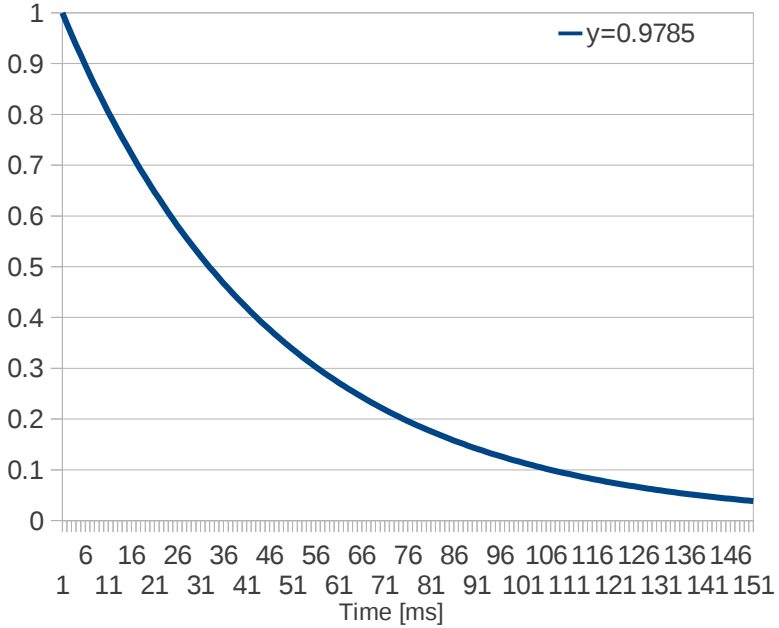
Load accumulation rate

- For some workloads tracked load saturates too fast and leads to unnecessary task migrations.
- Extending the tracked load history reduces tracked load variations due to sudden changes in the load characteristics.
- Increasing the y factor in the load expression decreases the load accumulation and decay rates.



$$load = \frac{u_0 + u_1 \cdot y + u_2 \cdot y^2 + \ldots + u_n \cdot y^n}{1024 + y + y^2 + \ldots + y^n + 1}$$

$$y < 1, 0 \leqslant u < 1024$$

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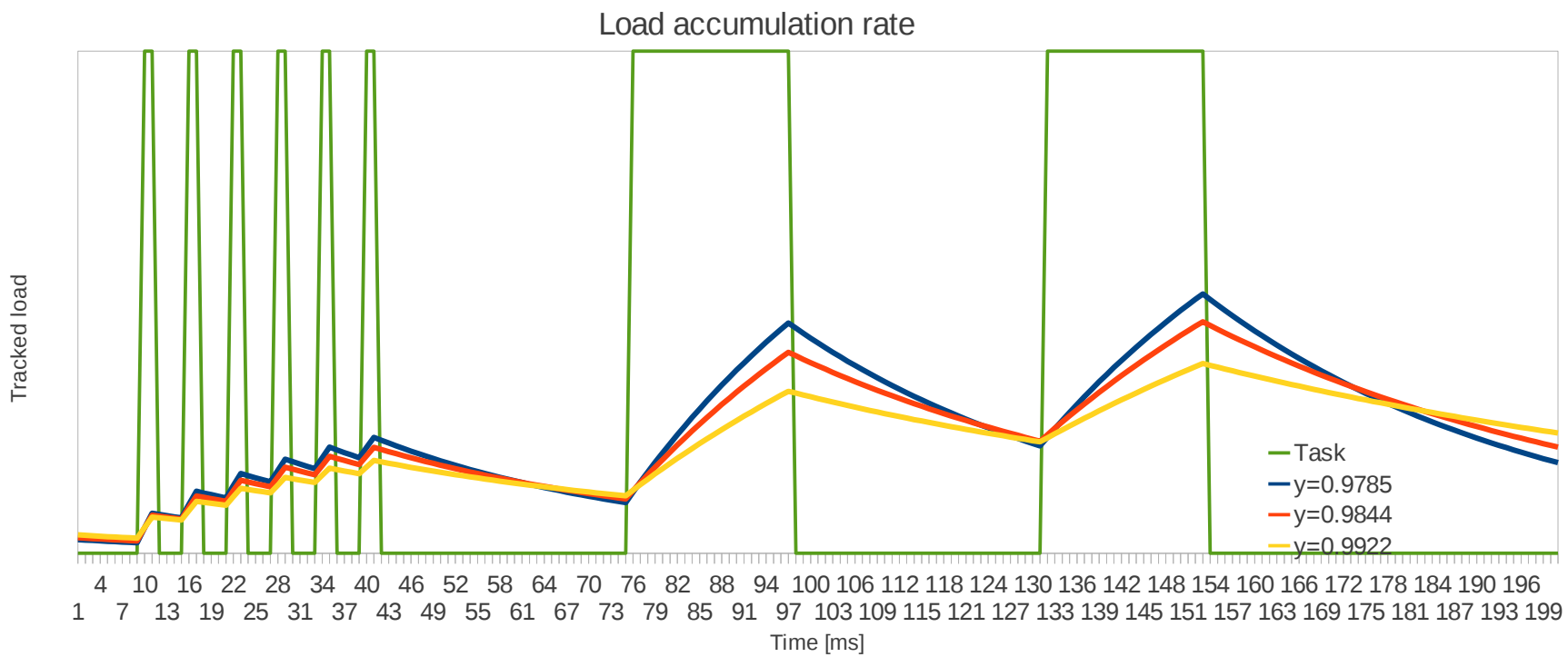
Load accumulation rate

- Increasing y leads to a more conservative tracked load
  - Should lead to less up/down migrations
  - Increases up/down migrations delay for tasks that needs to be migrated.



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MP – Top Issues

- Spurious wakeups
  - A15s are woken up by scheduler ticks (mainly)
  - Workqueues
  - Timers
  - RCU
- cpu wakeup prioritisation
  - Pick the cheapest target cpu
- Global balancing
  - Spread load to A7s when A15s are overloaded
  - Pack vs. spread
- Cluster aware cpufreq governors

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Questions?

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